

IN THE SPECIFICATION

Please replace the paragraph beginning at page 6, line 23, with the following paragraph:

According to still another aspect of the invention, there is provided a magnetic random access memory comprising a memory cell array of hierarchical bit line scheme in which cross-point memory cells that exhibit a magnetoresistive effect are laid out in a matrix, and a read bit line to be used in a data read mode is constituted by a main bit line and a sub bit line, connection means for selectively connecting a word line connected to a cross-point memory cell to be selected to select the memory cell to one of first and second potential supply sources which are different from each other, and control means for controlling the connection means to selectively connect the word line and to set the a further word line in an electrical electrically floating state [(.]], wherein the control means comprises first and second row decoders and word line drivers to set a potential of the word line in the read mode, and when the connection means is deactivated by the first and second row decoders and word line drivers, the further word line is set in the electrically floating state.

Please add immediately after the paragraph beginning at page 6, line 23, the following two new paragraphs:

According to still another aspect of the invention, there is provided a magnetic random access memory comprising a memory cell array of hierarchical bit line scheme in which cross-point memory cells that exhibit a megnetoresistive effect are laid out in a matrix, and a read bit line to be used in a data read mode is constituted by a main bit line and a sub bit line, connection means for selectively connecting a word line connected to a cross-point memory cell to be selected to one of first and second potential supply sources which are different from each other, and control means for controlling the connection means to selectively connect the word line and to set a further word line in an electrically floating sate,

wherein the control means comprises a row decoder and word line driver to set a potential of the word line in the read mode, and when the connection means is deactivated by the row decoder and word line driver, the further word line is set in the electrically floating state, and the connection means comprises first and second selection circuits which connect the word line to the first and second potential supply sources on the basis of an output signal from the row decoder and word line driver, each of the first and second selection circuits being constituted by an NMOS transistor, and each NMOS transistor is controlled by the output signal from the row decoder and word line driver.

According to still another aspect of the invention there is provided a magnetic random access memory comprising a memory cell array of a hierarchical bit line scheme in which cross-point memory cells that exhibit a magnetoresistive effect are laid out in a matrix, and a read bit line to be used in a data read mode is constituted by a main bit line and a sub bit line, connection means for selectively connecting a word line connected to a cross-point memory cell to be selected to one of first and second potential supply sources which are different from each other, and control means for controlling the connection means to selectively connect the word line and to set a further word line in an electrically floating state, wherein the control means comprises a row decoder and word line driver to set a potential of the word line in the read mode, and when the connection means is deactivated by the row decoder and word line driver, the further word line is set in the electrically floating state, and the connection means comprises first and second selection circuits which connect the word line to the first and second potential supply sources on the basis of an output signal from the row decoder and word line driver, the first selection circuit being constituted by a PMOS transistor, and the second selection circuit being constituted by an NMOS transistor, and each PMOS and NMOS transistor is controlled by the output signal from the row decoder and word line driver.

Please replace the paragraph beginning at page 9, line 20, with the following corrected paragraph:

FIG. 1 is a block diagram showing the main part of a magnetic random access memory (MRAM) according to the first embodiment of the present invention. The present invention is related to a read operation. For the sake of simplicity, FIG. 1 shows the core portion of the read system and does not illustrate the core portion of the write system. Cross-point memory cells MC11 to MC48 each constructed by an MTJ element are arranged in a plurality of (two) memory cell blocks (cell units). One terminal of each ~~to cross-point~~ memory cells MC11 to MC14, MC21 to MC24, MC31 to MC34, and MC41 to MC44 in the first memory cell block is connected by fours to a corresponding one of sub bit lines SBL1, SBL3, SBL5, and SBL7 serving as common nodes. One terminal of each ~~to cross-point~~ memory cells MC15 to MC18, MC25 to MC28, MC35 to MC38, and MC45 to MC48 in the second memory cell block is connected by fours to a corresponding one of sub bit lines SBL2, SBL4, SBL6, and SBL8 serving as common nodes. The sub bit lines SBL1 to SBL8 are respectively connected, for each column, to main bit lines MBL1 to MBL4 through the current paths of select MOS transistors Q1 to Q8 each functioning as a select switch (switch circuit). That is, as a cell unit selection signal, a high-level gate signal is supplied to one of the select MOS transistors Q1 to Q8 of the sub bit lines SBL1 to SBL8 including a selected cell. In other words, when a select line SS1 or SS2 is changed to a high potential, a specific one of the sub bit lines SBL1 to SBL8 can be selectively connected to a corresponding one of the main bit lines MBL1 to MBL4 for each cell unit.